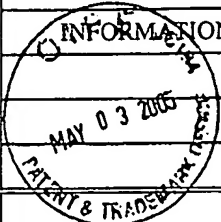
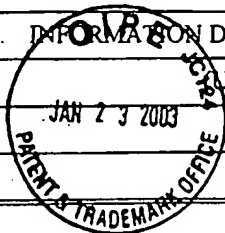
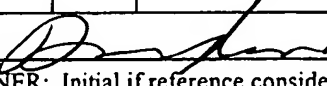


U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute PTO Form 1449				NS-5127 US		10/054,653	
				Applicant(s)		Confirmation No.	
				Constantin Bulucea		9448	
				Filing Date		Group	
				January 18, 2002		2814	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
Foreign Patent Documents							
		Document	Date	Country	Class	Subclass	Translation
	AL						Yes No
	AM						
	AN						
	AO						
	AP						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
DR	AQ	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOC's," <u>IEDM Technical Digest</u> , December 2001, pages 22.6.1 - 22.6.7					
	AR						
	AS						
Examiner <i>[Signature]</i>		Date Considered <i>9/13/05</i>					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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(Use several sheets if necessary)					Constantin Bulucea		9448	
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U.S. Patent Documents								
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
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DF	AC	6,100,770	08/00	Litwin et al.	331	117 FE		
DF	AD	6,166,404	12/00	Imoto et al.	257	279		
	AE							
Foreign Patent Documents								
							Translation	
	Document	Date	Country	Class	Subclass	Yes	No	
AF	6-61446	03/1994	Japan				X	
AG								
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	AI	Grove, <u>Physics and Technology of Semiconductor Devices</u> (John Wiley & Sons), 1967, pp. 263 - 305.						
	AJ	Grove, et al., "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon <i>p-n</i> Junction," <u>IEEE Trans. Electron Devices</u> , vol. ED-14, 1967, pp. 157 - 162.						
	AK	Grove, et al., "Surface Effects on <i>p-n</i> Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," <u>Solid-State Electronics</u> , Vol. 9, 1966, pp. 783 - 806.						
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	AM	Lee, <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> (Cambridge Univ. Press), 1998, pp. 37 - 41 and 504 - 514.						
	AN	McMahon, et al., "Voltage-Sensitive Semiconductor Capacitors," <u>1958 IRE Wescon Conf. Rec.</u> , Part 3, 19 - 22 August 1958, pp. 72 - 82.						
DF	AO	Moll, "Variable Capacitance With Large Capacity Change," <u>IRE Wescon Conf. Rec.</u> , Vol. 3, 1959, pp. 32 - 36.						
Examiner <i>[Signature]</i>		Date Considered 9/3/05						
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	AD							
	AE							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AF							
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	AM	Svelto, et al., "A Three Terminal Varactor for RF IC's in Standard CMOS Technology," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, 2000, pp. 893 - 895.						
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